

## ACCELERATING TEST VALIDATION AND DEBUG OF HIGH SPEED SERIAL INTERFACES%0A

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the rudimentary background information on high-speed serial interface standards. The chapter then enumerates the challenges that we are facing in high-speed serial interface testing, validation and debugging, and finally outlines our solutions.

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Accelerating Test, Validation and Debug of High Speed Serial Interfaces provides innovative test and debug approaches and detailed instructions on how to arrive to practical test of modern high-speed interfaces. Accelerating Test, Validation and Debug of High Speed Serial Interfaces first proposes a new algorithm that enables us to perform receiver test more than 1000 times faster. Then an under-sampling based transmitter test scheme is presented. The scheme can accurately extract the

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High-Speed Serial Interface (HSSI) devices have become widespread in communications, from the embedded to high-performance computing systems, and from on-chip to a wide haul. Testing of HSSIs has been a challenging topic because of signal integrity issues, long test time and the need of expensive

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