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This book addresses various issues for designing SRAM memory cells for advanced CMOS technology. To study LSI design, SRAM cell design is the best materials subject because issues about variability, leakage and reliability have to be taken into account for the design.

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1.2 Memory Cell Design Techniques and Array Design Techniques There are a lot of issues to obtain low power, reliable, and small cell size 6T memory cell. Since the 6T SRAM cell size is scaled by Moore s law, the feature size of transistors in 6T cell is also reduced by Moore s law. Supply voltage of 6T cell is also reduced as the feature size is reduced. Variation in the transistors

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