

## LOW POWER HIGH SPEED ADCS FOR NANOMETER CMOS INTEGRATION

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describes a 1.2 V, 52 mW, 210 MS/s, 10-bit ADC in 130 nm digital CMOS for appli- cation to digital (low) IF receivers, whose advantage over the direct-conversion as a highly integrated receiver architecture has been shown [33,35].

Low-Power High-Speed Adcs For Nanometer Cmos Integration

Low-Power High-Speed ADCs for Nanometer CMOS Integration ABC Dr. Zhibeng Cao Asst. Prof. Shouli Yan University of Texas, Austin Cockrell School of Engineering Dept. Electrical & Computer Engineering 1 University Station Austin TX 78712 ACES Bldg. USA [email protected] [email protected] ISBN 978-1-4020-8449-2 e-ISBN 978-1-4020-8450-8

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